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(19) (CA) **CANADIAN PATENT** (12)

(54) Integrated Semiconductor Circuit with Bipolar Transistor Structure, and a Fabrication Method Thereof

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ABSTRACT OF THE DISCLOSURE

The invention relates to an integrated semiconductor circuit with bipolar transistor structure, in which the emitter region as well as the base region and the collector contact region are produced by out-diffusion of a metal silicide layer provided with a respective doping substance and deposited directly on the substrate. The metal silicide layer structures provided with the respective doping, using in particular silicides of the metals tantalum, titanium, tungsten or molybdenum, serve as additional wiring planes and permit a higher density and a very low-resistance contacting structure.

CLAIMS

What is claimed is:

1. In an integrated semiconductor circuit with bipolar transistor structure, in which an emitter region as well as a base region in a silicon semiconductor substrate are produced by out-diffusion of a doped layer structure deposited directly on the substrate and serving as an additionalwiring plane, the improvement wherein said layer structure serving as wiring plane comprises a doped silicide of a metal compound of a high melting point.

2. Integrated semiconductor circuit with bipolar transistor structure according to claim 1, wherein said doped silicide of a metal includes a silicon excess in comparison to the disilicide stoichoimetry.

3. Integrated semiconductor circuit with bipolar transistor structure according to claim 1, wherein said metal compound may include the silicides of the metals tantalum, titanium, tungsten or molybdenum.

4. Integrated semiconductor circuit with bipolar transistor structure according to claim 2, wherein said metal compound may include the silicides of the metals tantalum, titanium, tungsten or molybdenum.

5. Integrated semiconductor circuit with bipolar transistor structure according to claim 1, wherein the layer of said metal silicide is 150 to 300 nm, preferably 200 nm thick.

6. Integrated semiconductor circuit with bipolar transistor structure according to claim 2, wherein the layer of said metal silicide is 150 to 300 nm, preferably 200 nm thick.

7. Integrated semiconductor circuit with bipolar transistor structure according to claim 3, wherein the layer of said metal silicide is 150 to 300 nm, preferably 200 nm thick.

8. Integrated semiconductor circuit with bipolar transistor structure according to claim 4, wherein the layer of said metal silicide is 150 to 300 nm, preferably 200 nm thick.

9. Method for producing npn bipolar transistor structure, in which an emitter region as well as a base region in a semiconductor substrate are produced by out-diffusion of a doped layer structure deposited directly on said substrate and serving as an additional wiring plane said method comprising the steps of:

a) defining the active areas of the structure by producing n^+-doped zones in a p-doped silicon substrate by masked ion implantation;

b) applying an epixtaxial n-doped layer on the n^+-doped zones;

c) masked etching of an insulation trench in the region between the n^+-doped zones;

d) producing the insulation oxide in the region of the insulation trench;

e) n^+-depth diffusing of a collector zone after a layer which masks the other regions has been applied;

f) detaching the masking layer for the collector depth diffusion and over-etching the substrate surface;

g) whole-area depositing of a first metal silicide layer admixed with p-doping substances, silicon being present in excess;

h) structuring of the p-doped silicide layer in the base zone of the transistor;

i) forming the base with p-doping ions after producing the mask for the base implantation;

j) out-diffusing the p-doping substances from the silicide base contact region;

k) executing an oxidation process;

l) performing an anisotropic dry etching process to remove the oxide layer in the emitter and collector terminal zones;

m) whole-area depositing of a second metal silicide layer provided with n-doping substances;

n) structuring of the second n-doped silicide layer in the emitter region and collector contact region (12), the structures overlapping the structures of the first metal silicide layer;

o) out-diffusing of the n-doping substances from the second silicide layer to form the emitter zone;

p) whole-area depositing of an insulation layer acting as intermediate oxide;

q) opening of the contacts to the p-doped regions of the first metal silicide layer and to the n-doped regions of the second metal silicide layer; and

r) metallizing and structuring the outer metal conductor track plane.

10. Method according to claim 9, wherein between process steps g) and h) the step of depositing an oxide layer which is structured with the first silicide layer such that a slight SiO_2 overhang is formed is included.

11. Method according to claim 9, wherein between process steps g) and h) an oxide layer is deposited which is structured with the first silicide layer and that instead of process step k) an oxide layer is deposited from the vapor phase.

12. Method according to claim 9, wherein for said silicide in process step g) and in process step m) a silicide of one of the metals tantalum, titanium, tungsten or molybdenum may be used.

13. Method according to claim 10, wherein for said silicide in process step g) and in process step m) a silicide of one of the metals tantalum, titanium, tungsten or molybdenum may be used.

14. Method according to claim 11, wherein for said silicide in process step g) and in process step m) a silicide of one of the metals tantalum, titanium, tungsten or molybdenum may be used.

15. Method according to claim 9, wherein boron is used for the doping of the first metal silicide layer (process step g) and arsenic is used for the doping of the second metal silicide layer (10) (process step m).

16. Method according to claim 10, wherein boron is used for the doping of the first metal silicide layer (process step g) and arsenic is used for the doping of the second metal silicide layer (10) (process step m).

17. Method according to claim 11, wherein boron is used for the doping of the first metal silicide layer (process step g) and arsenic is used for the doping of the second metal silicide layer (10) (process step m).

18. Method according to claim 9, wherein aluminum is used as metallization material for the outer metal conductor track plane according to process step r).

19. Method according to claim 10, wherein aluminum is used as metallization material for the outer metal conductor track plane according to process step r).

20. Method according to claim 11, wherein aluminum is used as metallization material for the outer metal conductor track plane according to process step r).

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BACKGROUND OF THE INVENTION

This invention relates to an integrated semiconductor circuit with a bipolar transistor structure in which the emitter region as well as the base region on the silicon semiconductor substrate are produced by out-diffusion of a doped layer structure deposited directly on the substrate and which serves as an additional wiring plane. The invention also relates to a method for the fabrication of the semiconductor device.

The smallest possible dimensions of bipolar transistors are determined by the relatively large metallization raster, since from the metal conductor track plane contacts must be produced to the emitter and collector zones as well as to the base zone.

Many attempts have been made to alleviate the wiring problem for example by a polysilicon wiring, as described in IEEE Trans. Electron. Devices, Vol. Ed-27, No. 8, August 1980, at pages 1379 to 1384 in an article by D.D. Tang et al, or by a polyzide wiring as described in IEEE Trans. Electron. Devices, Vol. ED-27, No. 8, August 1980, at pages 1385 to 1389 in an article by Y. Sasaki et al. Polysilicon wirings, however, have relatively high resistance and result in high series resistances. Since, as a rule, with this procedure the emiter is diffused out of the polysilicon, and the n^+ and p^+ dopings diffuse one into the other, there results moreover a high emitter-base capacitance, whereby the frequency response is adversely affected. The application published in Sasaki's article of a wiring consisting of molybdenum silicide does indeed reduce the wiring resistance relative to the polysilicon wiring considerably. But the method for producing this type of wiring is very costly because of the required masks.

SUMMARY OF THE INVENTION

It is, therefore, an object of the invention to disclose an integrated circuit with bipolar transistor structures in which the contacting and joining of the base, emitter and collector zones is independent of the metallization pitch and therefore makes possible a higher packing density. Moreover, the series resistance to the base zone is to be reduced.

It is also an object of the invention to provide a simpler method for the production of the circuit through mask-saving process steps.

The solution of this problem according to the invention is characterized in that the layer structure serving as wiring plane consists of a doped silicide of a metal of high melting point. Included under the scope of the invention is the idea that the metal silicide compound has an excess of silicon in comparison to the stoichiometry of the compound, to permit reoxidation without consumption of silicon from the substrate. Preferably the compound consists of a silicide of the metals tantalum, tungsten, molybdenum or titanium. The layer thickness of the metal silicide structure ranges from 150 to 300 nm, preferably about 200 nm.

The invention also provides a method for producing npn bipolar transistor structure, in which an emitter region as well as a base region in a semiconductor substrate are produced by outdiffusion of a doped layer structure deposited directly on said substrate and serving as an additional wiring plane said method comprising the steps of:

a) defining the active areas of the structure by producing n^+-doped zones in a p-doped silicon substrate by masked ion implantation;

b) applying an epixtaxial n-doped layer on the n^+-doped zones;

c) masked etching of an insulation trench in the region between the n^+-doped zones;

d) producing the insulation oxide in the region of the insulation trench;

e) n^+-depth diffusing of a collector zone after a layer which masks the other regions has been applied;

f) detaching the masking layer for the collector depth diffusion and over-etching the substrate surface;

g) whole-area depositing of a first metal silicide layer admixed with p-doping substances, silicon being present in excess;

h) structuring of the p-doped silicide layer in the base zone of the transistor;

i) forming the base with p-doping ions after producing the mask for the base implantation;

j) out-diffusing the p-doping substances from the silicide base contact region;

k) executing an oxidation process;

l) performing an anisotropic dry etching process to remove the oxide layer in the emitter and collector terminal zones;

m) whole-area depositing of a second metal silicide layer provided with n-doping substances;

n) structuring of the second n-doped silicide layer in the emitter region and collector contact region (12), the structures overlapping the structures of the first metal silicide layer;

o) out-diffusing of the n-doping substances from the second silicide layer to form the emitter zone;

p) whole-area depositing of an insulation layer acting as intermediate oxide;

q) opening of the contacts to the p-doped regions of the first metal silicide layer and to the n-doped regions of the second metal silicide layer; and

r) metallizing and structuring the outer metal conductor

track plane.

Other features and advantages of the invention will be apparent from the following description of the preferred embodiments and from the claims.

For a full understanding of the present invention, reference should now be made to the following detailed description of the preferred embodiments of the invention.

BRIEF DESCRIPTION OF THE DRAWINGS

Figs. 1 to 3 are sectional views of the integrated semiconductor incorporating bipolar structure in various stages of completion.

DETAILED DESCRIPTION

The process sequence for the production of a circuit with a bipolar transistor according to the invention will be described more specifically with reference to Figs. 1 to 3. In the Figs. only the process steps essential to the invention are illustrated in sectional views. Like parts are marked with the same reference symbols.

Fig. 1: On a monocrystalline, p-doped (100)-oriented silicon substrate wafer 1 having a specific resistance of 10 Ohm cm, the active areas of the circuit are defined by producing n^+-doped zones 2 by masked ion implantation. Then, by an epitaxial deposition method, an n^--doped silicon layer 3 having a specific resistance of 2 Ohm cm is applied on the n^+-doped zones 2 and the insulation trench is etched by means of a mask covering the active areas 2 (not shown in the Fig.). Thereafter the insulation oxide 4 is produced in the area of the insulation trench. Then, after applying a layer which masks the other regions, the n^+ depth diffusion 5 is carried out in the collector zone of the bipolar transistor. After removal of the mask for the collector depth diffusion 5 the substrate surface is etched over the whole area. Then follows the whole-area deposition of a tantalum silicide layer 7 admixed with boron (first silicide layer) in a layer thickness of 200 nm, silicon being present in excess (Ta:Si $<$ 1:2). To define the base contact region (6), this $TaSi_2$ layer 7 is provided with an oxide layer 8 to reduce the overlap capacitances and to prevent the out-diffusion of boron, and it is structured with the oxide layer 8 as illustrated in Fig. 1. After the production of an implantation mask for the base implantation (6), the base 6 is implanted with boron ions, whereupon the boron is diffused out of the tantalum silicide layer 7 at 800 to 1000°C. In so doing, the base implantation is also activated. There is formed the device shown in Fig. 1 with the p^+-diffused base contact zone marked with the reference symbol 9 and the base marked 6.

Fig. 2: After execution of an oxidation process (reoxidation of the $TaSi_2$, excess silicon SiO_2 being formed), the oxide layer is removed in the emitter zone (11) and in the collector contact area (12) by an anisotropic dry etching process, SiO_2 being left at the silicide edges. On the exposed emitter and collector contact terminal areas, arsenic-doped tantalum silicide(10)(second silicide layer) is deposited by sputtering of an arsenic-doped tantalum silicide target and is structured as can be seen from Fig. 2. The first silicide layer 7 is overlapped by the second silicide layer 10. For emitter formation (zone 11) arsenic is then diffused out of the tantalum silicide layer 10 at 800-1000°C. Simultaneously the diffused n^+-collector contact terminal 12 is formed.

Fig. 3: Shows the finished bipolar transistor structure after an insulation layer 13 acting as intermediate oxide has been produced. The finished structure is shown with the contacts to the boron-doped areas of the first tantalum silicide layer 7 (p^+ base 9) and to the arsenic-doped areas of the second tantalum silicide layer 10 (n^+ collector zone 12 or emitter 11) opened. The completed metallization with aluminum contact 14 and 15 are also shown.

The advantage of the invention over known bipolar transistor structures and their methods of fabrication resides in that with only one additional mask (contact between the first and second metal silicide) one obtains two low-resistance almost independent wiring planes (7 and 10) which, in particular, as cross couplings in static memory cells, permit a higher packing density.

In addition, the arrangment according to the invention results in the following advantages:

1. The contact metal/silicide (14 and 7, 15 and 10) has a resistance lower by one order of magnitude than the known contact metal/polysilicon.

2. The lead from the contact metal/silicide (14, 7) to the base (9) has a resistance lower by one order of magnitude than polysilicon.

3. In the critical etching of silicide (7, 10) on silicon it is easier, because of the different materials, to achieve an etching stop or respectively to carry out an endpoint control than when using polysilicon.

There has thus been shown and described a novel bipolar transistor structure and method therefor which fulfills all the objects and advantages sought therefor. Many changes, modifications, variations and other uses and applications of the subject invention will, however, become apparent to those skilled in the art after considering the specification and the accompanying drawings which disclose preferred embodiments thereof. All such changes, modifications, variations and other uses and applications which do not depart from the spirit and scope of the invention are deemed to be covered by the invention which is limited only by the claims which follow.

FIG 1

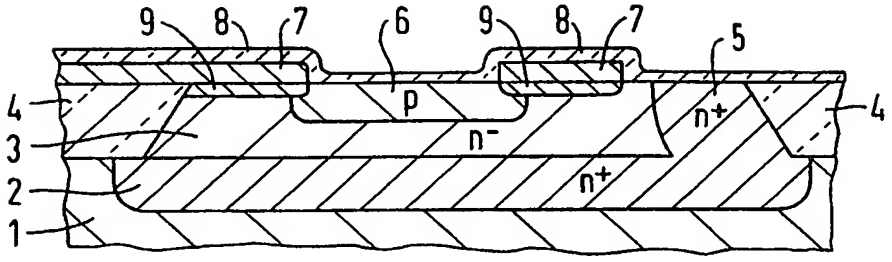


FIG 2

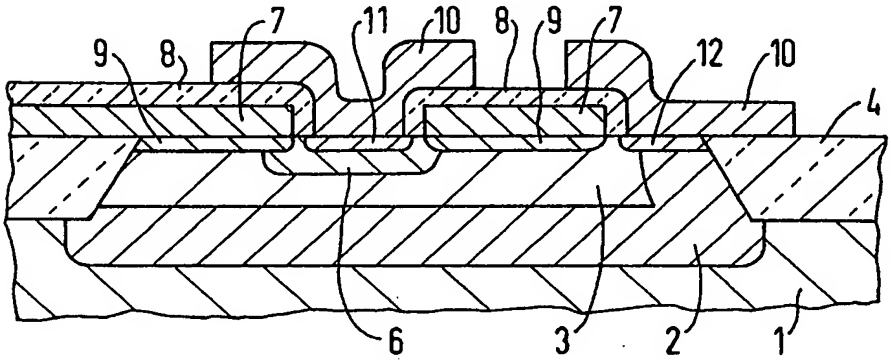
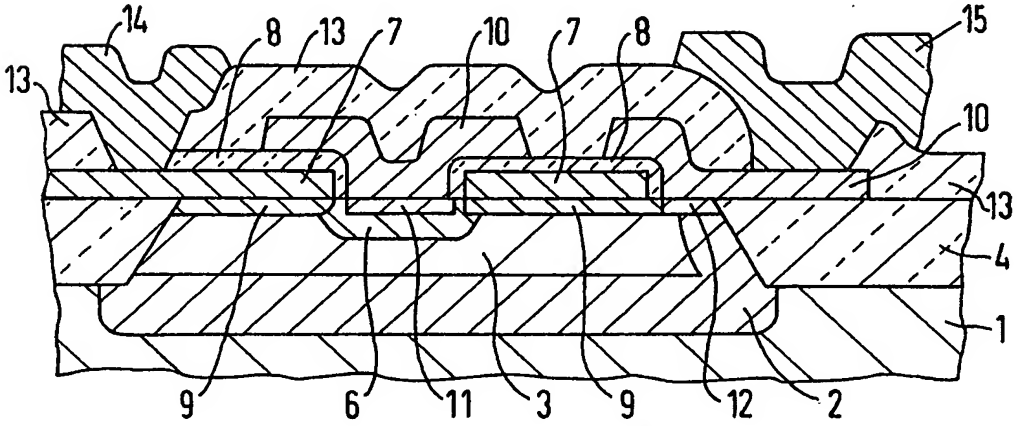


FIG 3



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